Laydu Singh Charitable Trust's (Regd.)
THAKUR COLLEGE OF ENGINEERING & TECHNOLOGY
Autonomous College Affiliated to University of Mumbai
Approved by All India Council for Technical Education(AICTE) and Government of Maharashtra(GoM)
Conferred Autonomous Status by University Grants Commission (UGC) for 10 years w.e.f. A.Y 2019-20
Amongst Top 200 Colleges in the Country Ranked 193rd in NIRF India Ranking 2019 in Engineering College category
• ISO 9001:2015, 14001:2015, 20001:2018 Certified • Programmes Accredited by National Board of Accreditation (NBA), New Delhi
• Institute Accredited by National Assessment and Accreditation Council (NAAC) Bangalore
Website : www.tcetmumbai.in
Estd. 2001

IN-SEMESTER EXAMINATION-I

S.E. (Semester-III)

SUBJECT – DIGITAL CIRCUIT DESIGN

Branch: IT
Div.: ALL
Duration: 60 Minutes

Date: 28/08/2024
Timing: 10:00 AM to 11:00 AM
Maximum Marks: 20

Instructions –

1. All questions are compulsory.
2. Assume suitable data wherever necessary and state the assumptions made.
3. Diagrams / sketches should be given wherever necessary.
4. Use of logarithmic table, drawing instruments and non-programmable calculators is permitted.
5. Figures to the right indicate full marks.

Q.1		Answer any 5 of the following questions	Marks	Course Outcomes	Learning Levels
	a.	Define two's complement number system with a suitable example.	2	1	U
	b.	Convert (103)10 into its equivalent octal number.	2	1	R
	c.	Define weighted and non-weighted codes	2	1	U
	d.	Use a combination of AND, OR, and NOT gates to implement a simple logic circuit for the expression **A.(B+C')**	2	2	A
	e.	f=ABC+BC'D+A'BC; Realize f using NAND gates only.	2	2	A
	f.	What are the main components of a Half-Subtractor, and what is its primary function?	2	3	R
	g.	Draw the K map for 2,3 & 4 Variable K map.	2	3	R
Q.2	a.	Convert the following expression in standard POS form: 1)f(A,B,C)=(A+B)(B+C) 2)f(P,Q,R)=(P+Q')(P+R)	5	2	AN
		OR			
	b.	Reduce the following Boolean expressions: **1) BC'D'+BCD' 2) (C'+B)(C+B).**	5	2	A
Q.3	a.	Compare and contrast the structure and function of a Half-Adder and a Full Adder. What are the key differences in their implementation and application?	5	3	A
		OR			
	b.	Design and implement 3-bit Gray to binary code converter.	5	3	A

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IN-SEMESTER EXAMINATION-II

S.E. (Semester-III)

SUBJECT – DIGITAL CIRCUIT DESIGN

Branch: IT
Div.: ALL
Duration: 60 Minutes

Date: 18/10/2024
Timing: 10:00 AM to 11:00 AM
Maximum Marks: 20

Instructions –

1. All questions are compulsory.
2. Assume suitable data wherever necessary and state the assumptions made.
3. Diagrams / sketches should be given wherever necessary.
4. Use of logarithmic table, drawing instruments and non-programmable calculators is permitted.
5. Figures to the right indicate full marks.

Q.1		Answer any 5 of the following questions	Marks	Course Outcomes	Learning Levels
	a.	Write the characteristic equation of a JK flip-flop.	2	4	U
	b.	What is disadvantage of S-R Flip Flop.	2	4	U
	c.	Which type of shift register is used to convert Serial Data into parallel form?	2	5	U
	d.	Differentiate between SISO and SIPO registers	2	5	A
	e.	What is the primary difference between asynchronous and synchronous counters in digital logic?	2	6	U
	f.	What will be the state of a 2-bit synchronous down counter starting from 11 after two clock pulses?	2	6	U
	g.	Discuss the relationship between number of flip flops required and number of states of counter	2	6	U
Q.2	a.	Draw and explain the operation of S-R Latch using NOR gate	5	4	A
		OR			
	b.	Compare combination circuits with sequential circuits	5	4	AN
Q.3	a.	Explain the bidirectional shift register and its significance in digital circuits.	5	5	A
		OR			
	b.	Describe the construction and operation of a 4-bit parallel register.	5	5	AN

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29 NOV 2024

END SEMESTER EXAMINATION, DEC 2024
S.E. SEMESTER III (CBCGS-HME 2023)

Branch:	**IT**	**Q.P. Code:**	**ED243ITR5S3-1**
Subject:	**Digital Circuit Design**	**Duration:**	**2 hours**
Subject Code:	**ESC-IT 301**	**Max. Marks:**	**60**

Instructions:
1. **All sections are compulsory**
2. **Figures to the right indicate full marks.**
3. **Assume suitable data if necessary and state the assumptions clearly.**

Section-I	**Short Answer Questions (Answer any 05 questions out of 06) (Fundamental, Core Types)**				**(10 Marks)**
Q. No.		**Marks**	**CO**	**RBT Level**	**PI**
1	Define signed magnitude Number system.	2	1	U	2.7.2
2	What do you mean by literals?	2	2	A	2.6.4
3	Define full subtractor.	2	3	R	2.7.2
4	Draw truth table, symbol of Clocked T Flip flop & Clocked D Flip flop.	2	4	U	3.5.1
5	What is a bidirectional shift register?	2	5	U	2.8.2
6	What will be the state of a 2-bit synchronous down counter starting from 11 after two clock pulses?	2	6	U	1.2.1
Section-II	**Descriptive Answer Questions (Answer any 04 out of 06) (Descriptive, Comprehension Types)**				**(20 Marks)**
1	State the procedure to convert decimal number to binary numbers.	5	1	A	2.8.2
2	Design a Boolean function in POS form and convert it to SOP form. Use a specific example to illustrate the entire process.	5	2	A	2.8.1
3	Design half subtractor using basic gates.	5	3	A	2.7.2
4	Compare combination circuits with sequential circuits.	5	4	AN	2.8.1
5	Compare the working of a Ring Counter with that of a Twisted Ring Counter.	5	5	A	2.8.2
6	Design a ripple counter using JK flip flop: Divide-by-5.	5	6	A	1.2.1
Section-III	**Long Answer Question (Answer any 03 out of 05) (Application, Analytical, Evaluation, Design Type)**				**(30 Marks)**
1	Explain the Demorgan's theorems in Boolean algebra and prove them.	10	2	A	2.8.2
2	Describe the steps involved in implementing a BCD adder using the IC 7483. What corrections are necessary for BCD addition?	10	3	A	2.8.1
3	Draw and explain circuit diagram, truth table, symbol of Clocked S-R & J K Flip flop.	10	4	A	1.2.1
4	Analyze the role of shift registers in the design of counters and explain their significance in digital electronics.	10	5	AN	3.5.1
5	Design a 2-bit synchronous up/down counter and describe how to implement it with JK flip-flops.	10	6	AN	1.6.1