Website : www.tcetmumbai.in

Lagdu Singh Charitable Trust's (Regd.)
THAKUR COLLEGE OF
ENGINEERING & TECHNOLOGY
Autonomous College Affiliated to University of Mumbai
Approved by All India Council for Technical Education(AICTE) and Government of Maharashtra(GoM)
Conferred Autonomous Status by University Grants Commission (UGC) for 10 years w.e.f. A.Y 2019-20
Among Top 250 Colleges in the Country where NIRF India Ranking 2020 in Engineering College category
• ISO 9001:2015 [illegible] • Programmes Accredited by National Board of Accreditation (NBA), New Delhi
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IN-SEMESTER EXAMINATION-I

S.E. (Semester-IV)

SUBJECT – Computer Organization Architecture & Microprocessors

Branch: Information Technology
Div.: ALL
Duration: 60 Minutes

Date:10/03/2025
Timing: 02:00 TO 03:00 PM
Maximum Marks: 20

Instructions –

1. All questions are compulsory.
2. Assume suitable data wherever necessary and state the assumptions made.
3. Diagrams / sketches should be given wherever necessary.
4. Use of logarithmic table, drawing instruments and non-programmable calculators is permitted.
5. Figures to the right indicate full marks.

Q.1		Answer any 5 of the following questions	Marks	Course Outcomes	Learning Levels
	a.	List the flags in the 8086 microprocessor.	2	1	R
	b.	Describe the function of the ALU in a microprocessor.	2	1	U
	c.	Illustrate the role of the Data Bus in system communication.	2	1	U
	d.	State the purpose of MOV instruction in 8086 with example.	2	2	U
	e.	Explain the function of the PUSH and POP instructions in 8086.	2	2	U
	f.	Draw flow chart of Add and shift method of integer multiplication.	2	3	A
	g.	State the difference between restoring and non-restoring algorithm.	2	3	AN
Q.2	a.	Discuss the role of the instruction pointer (IP) in 8086 and its impact on program execution.	5	2	U
		OR			
	b.	With the help of neat diagram explain the architecture of 8086.	5	2	A
Q.3	a.	Multiply 13 with 12 using Add and shift method of integer multiplication.	5	3	AN
		OR			
	b.	Solve $(1117.125)_{10}$ using IEEE 754 floating point standard using double precision.	5	3	AN

ISE-1 March 2024

ESE 2024

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IN-SEMESTER EXAMINATION-II

S.E. (Semester-IV)

SUBJECT – Computer Organization Architecture & Microprocessors

Branch: Information Technology
Div.: ALL
Duration: 60 Minutes

Date:15/04/2025
Timing: 04:00 TO 05:00 PM
Maximum Marks: 20

Instructions –

1. All questions are compulsory.
2. Assume suitable data wherever necessary and state the assumptions made.
3. Diagrams / sketches should be given wherever necessary.
4. Use of logarithmic table, drawing instruments and non-programmable calculators is permitted.
5. Figures to the right indicate full marks.

Q.1		Answer any 5 of the following questions	Marks	Course Outcomes	Learning Levels
	a.	List different Hard wired Control unit methods.	2	4	R
	b.	Explain Instruction pipelining in short.	2	4	U
	c.	Differentiate between SRAM and DRAM.	2	5	U
	d.	State the purpose of cache memory.	2	5	R
	e.	Write short note on Peripheral device: Mouse	2	6	R
	f.	List advantages and disadvantages of Programmed I/O. (ESE 2024)	2	6	R
	g.	Write short note on Peripheral device: Keyboard	2	6	R
Q.2	a.	What is pipelining? Explain six stage instruction pipeline with suitable diagram. Compare Pipelining and Non-Pipelining.	5	4	A
		OR			
	b.	Differentiate between Hardwired and Micro programmed control unit.	5	4	AN
Q.3	a.	Discuss various characteristics of memory.	5	5	AN
		OR			
	b.	Draw and explain Memory Hierarchy.	5	5	A

ISE April 2024

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END SEMESTER EXAMINATION, MAY 2025
S.E. SEMESTER IV (CBCGS-HME 2023)

Branch:	**Information Technology (IT)**	**Q.P. Code:**	**E466RM252-1**
Subject:	**Computer Organization Architecture and Microprocessor**	**Duration:**	**2 hours**
Subject Code:	**ESC-IT-401**	**Max. Marks:**	**60**

Instructions: **1. All sections are compulsory**
2. Figures to the right indicate full marks.
3. Assume suitable data if necessary and state the assumptions clearly.

Section-I	**Short Answer Questions (Answer any 05 questions out of 06) (Fundamental, Core Types)**	**Marks**	**CO**	**RBT Level**	**PI**
1	Discuss the memory storage unit in detail.	2	1	U	1.6.1
2	Explain the function of the PUSH and POP instructions in 8086.	2	2	U	2.8.1
3	Draw Booth's multiplication algorithm flowchart.	2	3	A	3.8.3
4	List different Hard wired Control unit methods.	2	4	R	1.6.1
5	List Advantages and Disadvantages of Direct mapping.	2	5	R	1.6.1
6	What are major requirements for an I/O module?	2	6	R	1.6.1
Section-II	**Descriptive Answer Questions (Answer any 04 out of 06) (Descriptive, Comprehension Types)**				**(20 Marks)**
1	Discuss the bus structure of the system in detail with its types and diagram.	5	1	A	1.6.1
2	Describe the role of assembler directives in 8086 programming. Include examples of commonly used directives.	5	2	U	2.8.1
3	Solve (15.125)10 using IEEE 754 floating point standard using Single precision and double precision.	5	3	AN	2.8.1
4	Identify and explain the types of hazards that can occur in a pipeline.	5	4	U	1.6.1
5	Draw and explain Memory Hierarchy.	5	5	A	1.6.1
6	Describe working of Mouse. List types of Mouses.	5	6	A	1.6.1
Section-III	**Long Answer Question (Answer any 03 out of 05) (Application, Analytical, Evaluation, Design Type)**				**(30 Marks)**
1	Discuss the instruction set of the 8086 microprocessor and describe the types of data transfer instructions with examples.	10	2	U	2.8.1
2	Divide 11 by 2 using Restoring and Non- Restoring Division method.	10	3	AN	2.8.1
3	Illustrate Flynn's classification in detail.	10	4	A	1.6.1
4	Solve following problem with FIFO, LRU and Optimal page replacement method and find page hits and page faults.	10	5	AN	4.6.3

	Consider the following page references with frame size 3. 1,2,3,4,2,1,5,6,2,1,2,3,7,6,3,2,1,2,3,6,1,2,3,4,2				
5 ESE 2024 ESE 2024	Write notes on: a) Programmed I/O b) Interrupt driven I/O	10	6	R	1.6.1